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Buried centimeter-long micro- and nanochannel arrays in porous silicon and glass†

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We developed a simple process to fabricate deeply buried micro- and nanoscale channels in glass and porous silicon from bulk silicon using a combination of ion beam irradiation, electrochemical anodization and high temperature oxidation. The depth, width and length of these structures can be controllably varied and we successfully fabricated an array of centimeter-long buried micro- and nanochannels. This process allows densely packed, arbitrary-shaped channel geometries with micro- to nanoscale dimensions to be produced in a three-dimensional multilevel architecture, providing a route to fabricate complex devices for use in nanofluidics and lab-on-a-chip systems. We demonstrate the integration of these channels with large reservoirs for DNA linearization in high aspect ratio nanochannels.

1. Introduction

There has been increasing interest in nanofluidic systems as a result of their demonstrated unique bioanalytical capabilities in nanofluidic devices, including the ability to elongate single DNA molecules,[1–4] concentrate protein samples by more than four orders of magnitude,[5] and efficiently separate both large[6,7] and small[8] biomolecules. The fabrication of nanofluidic structures plays an essential role in bio-nanotechnology, including sequencing of large-scale genomic information and epigenetic profiling.[9–11] Various techniques have been reported to fabricate nanochannels, such as e-beam lithography, the step sidewall approach, CMOS processes, laser writing and nanoimprinting. However, flexible fabrication of long, stable nanochannels of sub-100 nm diameter is still challenging. To the best of our knowledge, the fabrication of multi-layer nanofluidic chips with 3D channel architecture with these essentially 2D writing technologies has been elusive despite their potential importance for versatile lab on chip designs.

Here we first review the use of porous silicon and glass in buried channel fabrication and applications. We then describe how our process is used for fabrication of buried micro- and nanochannels and nanoslits in porous silicon and glass directly from bulk silicon using high-energy ion beam irradiation. We also demonstrate the possibility of fabricating vertical and multilevel buried channels using this technique and the integration of these structures with reservoirs for DNA studies.

Porous silicon is a widely used material in biotechnology, micro- and nanofabrication, photonics, microreactors and microfluidics,[12,13] where the ability to machine surface microchannels, *e.g.* using laser induced oxidation,[14] is crucial. Such surface channels can subsequently be covered to provide shallow, buried channels using additional processing steps. Uses of porous silicon based channels include microreactor fabrication[15] and gas pre-concentration.[16] In biotechnology, porous silicon is used as the carrier matrix in conjunction with microstructured planar surfaces to increase the surface area for enzyme coupling.[17] In nanotechnology, ferromagnetic nanostructures can be incorporated in porous silicon channels,[18] patterned porous silicon substrates are used to generate interconnected networks of niobium nanowires,[19] and thin films of nanostructured porous silicon can be filled by capillary forces.[20] In photonics,[21] porous silicon waveguides have been fabricated for infrared wavelengths,[14,22] and hollow waveguides in Ta_2O_5 and SiO_2 films are described in ref. 22. The DIPS process (direct imprinting of porous substrates) uses porous silicon as an imprintable material for use in plasmonics, holography, and sensing.[23,24]

Micro- and nanofluidics[25–27] rely on the ability to fabricate small grooves and hollow channels as the basic building blocks of structures and devices, acting as connectors between valves and pumps, sensors,[28] separation columns for chromatography,[29,30] waveguides[31] or heat exchangers.[32,33] Polymers such as PDMS are widely used but have limitations when the channel diameter is reduced as they suffer from swelling which reduces the channel area or even completely closes it. Micromachined channels in electrically insulating and optically transparent materials such as glass and quartz have become more important.[34–37]

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Researchers have used them in DNA analysis.[38,39] Others have produced centimeter long sub 20 nm channels *via* nano-imprinting and subsequent etching,[40,41] while more recently Menard and Ramsey[42] have shown sub 5 nm nanochannels in quartz substrates. All of these techniques require a bonding process after channel fabrication. Furthermore, glass and quartz carry a negative surface charge, which has the advantage of net negatively charged biomacromolecules such as DNA being not electrostatically adsorbed.

Integrating complex three-dimensional micro/nanostructures, including channel networks, vertical connecting channels,[42] valves, sensors and actuators, into a single device is an important development for lab-on-a-chip systems; integrating various molecular biology operations relies on using biocompatible materials, which include porous silicon, glass and composites.[43] Glass substrates are robust and transparent but fabricating complex geometries comprising deeply buried channels and/or nanoscale channels, chambers and other geometries using existing methods is challenging. For example, femtosecond laser writing[44–46] and laser lithography[47] have shown flexibility in fabricating micro- and nanochannels but have limited resolution. In other fields, *e.g.* micro-optics and photonics, energy and medicine,[48] micro-patterned glass has an important role as a medium for optical transmission of waveguides, and also as a cladding material for silicon waveguides.

2. Fabrication process of buried channels

High-fluence, high-energy ion irradiation of p-type silicon alters the subsequent electrochemical anodization behavior, leaving solid silicon at the irradiated regions, while porous silicon is formed at the surrounding unirradiated regions.[49] Ion irradiation introduces lattice damage in the form of vacancy–interstitial pairs, some of which act as hole traps,[50–52] thereby reducing the density of free positive charge carriers along the irradiated trajectory. For high-fluence irradiation, regions become fully depleted of acceptors and take no part in anodization,[49,53,54] hence silicon machining using high-fluence ion irradiation enables the formation of micro- and nanoscale wires,[55,56] surface and three-dimensional patterning and fabrication of components such as waveguides for silicon photonics.[56–59]

We have recently observed the effects of diffusion current funneling induced by low-fluence ion irradiation,[58,60] resulting in a significant anodization current flowing into regions of reduced carrier density. Here we use this effect as a means of inducing a high anodization current to flow through ion irradiated end-of-range regions, *i.e.* the opposite effect of that observed at high fluences where current is excluded, enabling the fabrication of complex micro- and nanoscale buried channels in porous silicon and glass.

The first step is irradiation of p-type silicon with a low fluence of high-energy ions, usually protons or helium ions of energies of 100 keV to 2 MeV. These ions have a well-defined range in silicon between 0.5 and 50 μm depending on the incident energy. The focused beam remains well collimated, with little lateral scattering, except for close to the end-of-range depth (Fig. 1a), which was generated using SRIM (Stopping and Range of Ions in Matter).[61] Ion irradiation results in a small volume at the end-of-range depth being highly damaged, with the portion closer to the surface being damaged to a lesser extent. For 1 MeV protons, the maximum damage occurs at an end-of-range depth of ~15 μm, allowing a sub-surface distribution of reduced carrier density to be built up (Fig. 2a). The low-fluence irradiated wafers are electrochemically anodized in a solution of 24% HF (a 1 : 1 solution of HF (48%) : ethanol) for several minutes, depending on the required etch depth. During electrochemical anodization the hole current is funneled and concentrated into the lightly damaged end-of-range regions (see the inset in Fig. 2b); the combined effect of a locally increased current passing through a region of decreased carrier density results in highly porous silicon being selectively formed at the end-of-range regions, compared to the surrounding unirradiated silicon where lower porosity silicon is formed.

After anodization the sample is rinsed with ethanol and then with distilled water for 5 minutes. After a certain period of exposure of the anodized wafer to ambient conditions (typically three days), or by brief thermal oxidation, all remaining porous silicon is

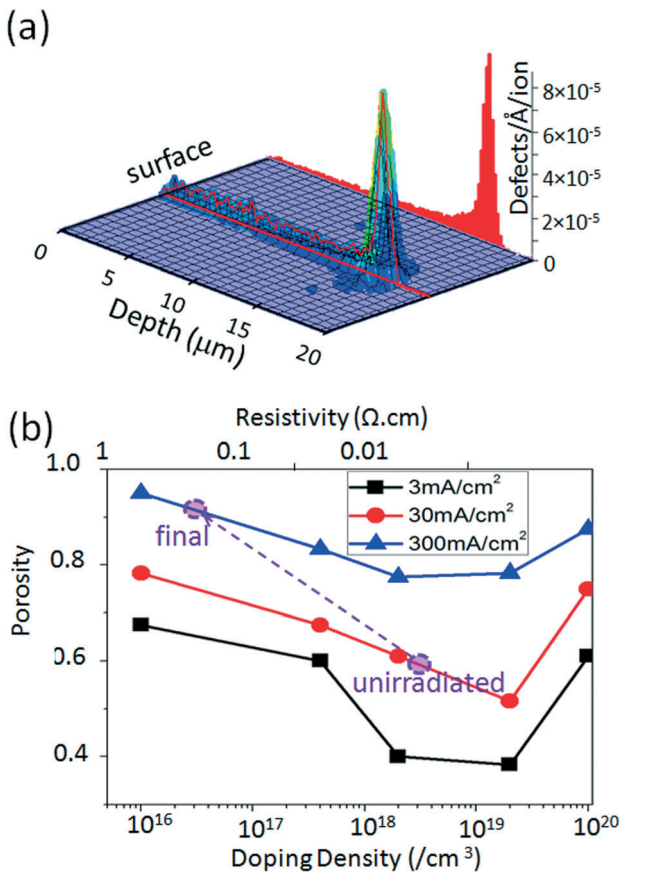

Fig. 1 (a) SRIM simulated plot of defect distribution *versus* depth of 1 MeV protons in silicon. The box size is 20 × 20 μm. (b) Anodized p-type silicon porosity *versus* wafer doping density at different anodization current densities [data from ref. 12].

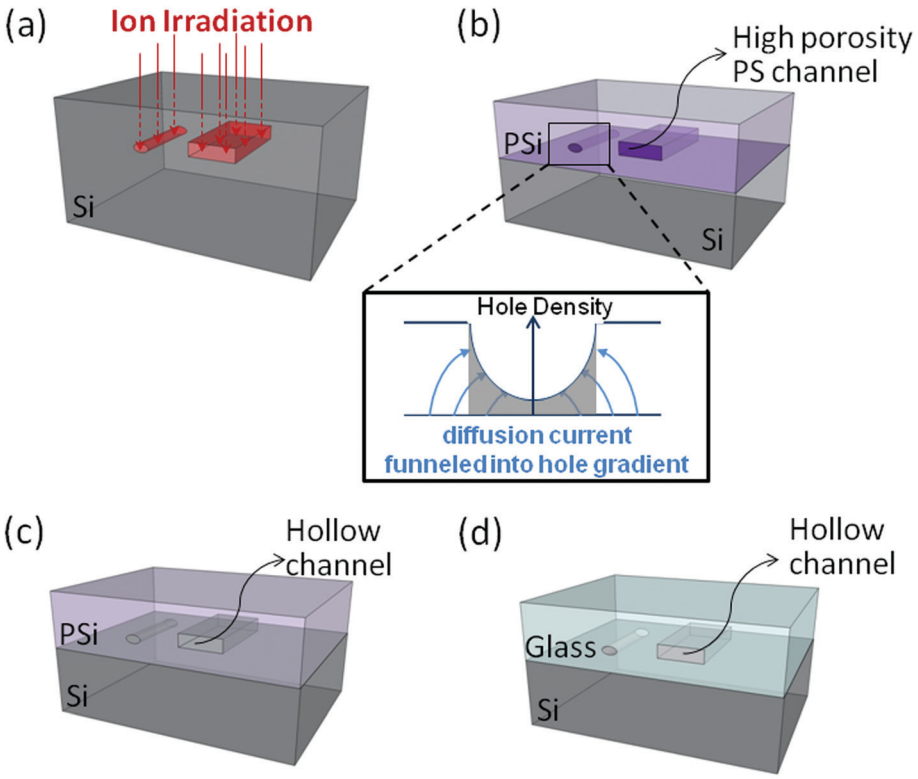

Fig. 2 Schematic of steps for making buried horizontal channels. (a) Low fluence irradiation of lines and extended areas, producing high defect concentration at the end-of-range depth. (b) Deep electrochemical anodization to produce a low porosity silicon matrix with high porosity end-of-range regions. The inset shows a schematic of current funneling into the end-of-range region during anodization. (c) Removal of highly porous silicon using dilute HF. (d) High temperature oxidation to convert remaining low porosity silicon into FOPS.

slightly oxidized. The oxide is easily removed by brief immersion in dilute hydrofluoric acid. Highly porous silicon at the end-of-range regions is completely removed by this process, while the lower porosity surrounding regions remain intact, resulting in buried channels in porous silicon (Fig. 2c). To fabricate buried channels in glass, a high temperature oxidation step (1000 °C for two hours) converts all remaining porous silicon into fully oxidized porous silicon (FOPS). Under optimized wafer anodization and oxidation conditions (described below) this forms a continuous volume of glass (Fig. 2d). By controlling the focused ion beam position, fluence and energy on the wafer surface within the target chamber of a nuclear microprobe,[62] any three-dimensional distribution of reduced carrier density may be built up.

An important aspect of this process is the choice of wafer resistivity, which determines whether irradiation and anodization can induce a sufficiently increased porosity at irradiated regions. Fig. 1b shows the final porosity of different resistivity p-type silicon after anodization; porosity generally increases with current density and with wafer resistivity (except for very highly doped wafers). A porosity of ~56% is optimum for converting porous silicon into FOPS,[53] where the volume expansion during incorporation of oxygen and formation of SiO_2 completely fills the voids in a porous silicon matrix, resulting in a continuous glass volume. A porosity higher than 56% means that there is not enough silicon present, so the final oxidized volume contains small voids. For a lower porosity the available space within the porous silicon is insufficient to allow sufficient volume expansion during oxidation, leading to strain and cracks in the final volume. The current density required to produce a final porosity of ~56% in 0.02 Ω cm p-type silicon (the choice of this resistivity is discussed below) as shown in Fig. 1b (purple circle, labeled 'unirradiated') is about 30 mA cm^{-2}. However, the small increase in porosity after the first oxidation step needs to be accounted for, so the porosity after anodization should be slightly lower than 56%. In practice, the relationship between porosity, oxidation temperature and volume expansion is more complex[63] but the above discussion serves as a useful guide.

We used ion irradiation to increase the resistivity (decrease the free carrier density) of a low resistivity p-type wafer to the point where highly porous regions are locally created during anodization. In low resistivity wafers, low porosity mesoporous silicon preferentially forms upon anodization, whereas in higher resistivity wafers, formation of higher porosity microporous silicon is more likely.[12] For example, in Fig. 1b a porosity of ~90%, (purple circle, labeled 'final') is produced at a region where ion irradiation locally increases the resistivity to ~0.5 Ω cm.[53] An anodization current density of 30 mA cm^{-2} flowing through the unirradiated wafer is funneled into and concentrated to ~300 mA cm^{-2} at the irradiated region, resulting in a much higher porosity compared to ~56% produced at the unirradiated region. Such a large increase in porosity can only

be induced in wafers with a resistivity of 0.01 to 0.05 Ω cm, where the porosity reaches a minimum for a given current density. A further advantage of using low resistivity wafers is that the resulting mesoporous silicon tends to have a low strain, allowing thick porous layers >100 μm to be produced without cracking. This is an important aspect in forming deeply buried channel arrays where cracking would lead to fluid leakage or defects in the optical properties of the channel array.

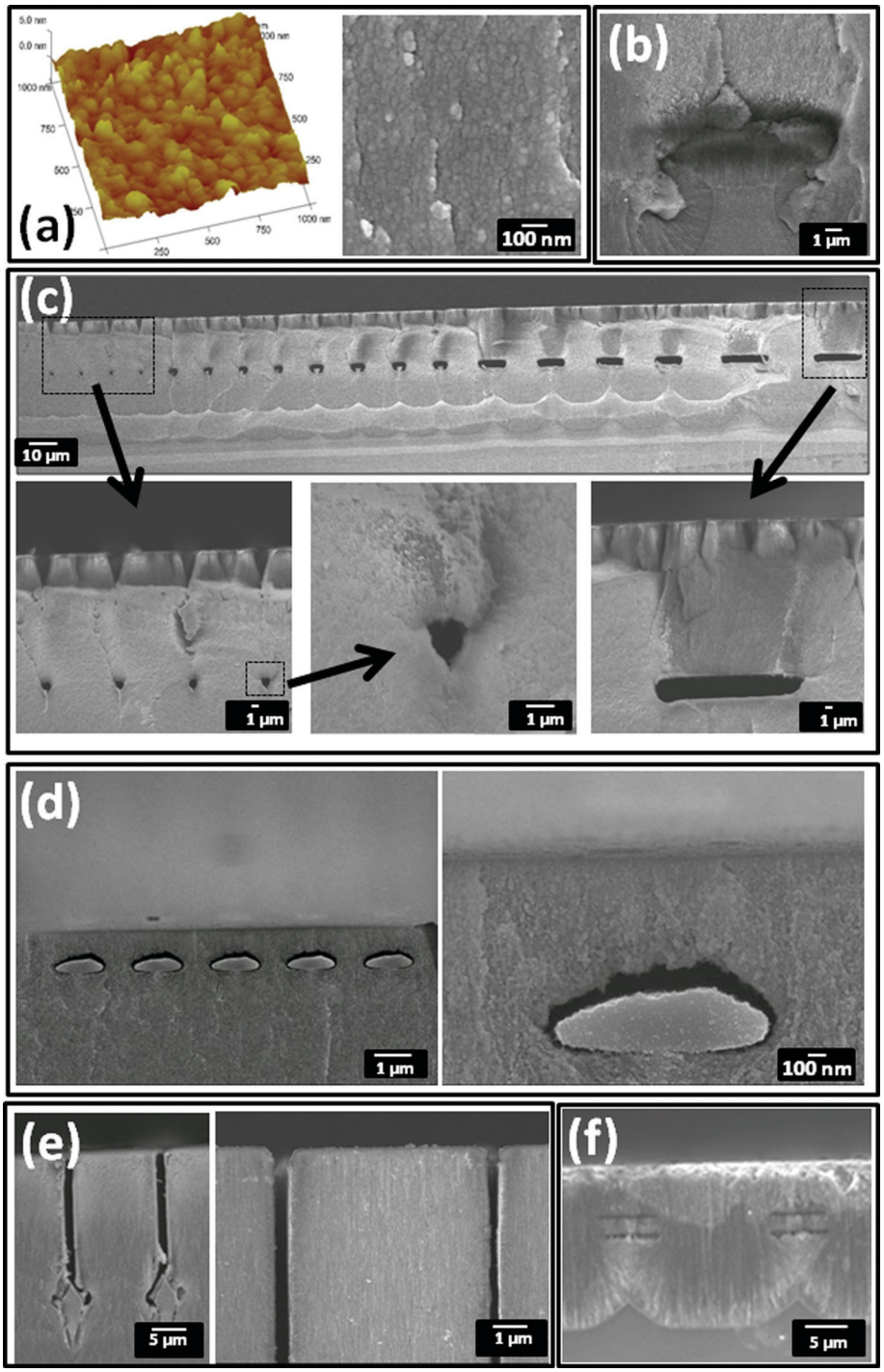

Fig. 3 (a) [Left] AFM image of the unirradiated oxidized porous silicon surface. [Right] Cross-section high magnification SEM image of the same sample. (b),(c) Cross-section SEM images of lines in porous silicon which were irradiated with 1 MeV protons over widths of 0.2, 3, 5, 10 and 17 μm from left to right, after anodization, with four adjacent lines irradiated in each case. (b) Before removal of highly porous regions; (c) low magnification of all lines after removal of highly porous silicon. The left-hand dashed box indicates the locations of the 0.2 μm width irradiation with a line fluence of $\Psi_l = 3 \times 10^{10}$ cm^{-1}. (d) 100 keV proton irradiation with a fluence of 1×10^{15} ions cm^{-2} over a width of 1 μm to fabricate buried high aspect ratio channels with a large core. (e) Vertical channels in porous silicon formed using 1 MeV protons. (f) Channels in porous silicon at different depths produced using different proton energies.

Fig. 3a shows some initial characterization results of an unirradiated, anodized silicon wafer after oxidation. The smooth glass silicon surface in the AFM (atomic force microscopy) image has a r.m.s. roughness of only 0.6 nm. SEM shows that the oxidized porous silicon comprises grains of typically 30 nm diameter.

3. Examples of fabricated channels

In Fig. 3b, c 500 μm long lines of width 0.2, 3, 5, 10 and 17 μm were irradiated with a focused beam of 1 MeV protons with an areal fluence of $\Psi_a = 3 \times 10^{14}$ cm^{-2} in a 0.02 Ω cm wafer. A line width of 0.2 μm is equivalent to a line fluence of $\Psi_l = 3 \times 10^{10}$ cm^{-1} [see the ESI† for definition and discussion of line fluence]. The wafer was then anodized at 25 mA cm^{-2} and cleaved for SEM imaging. The fluence is sufficient to reduce, but not fully deplete, the carrier density to the point where solid cores are formed after anodization. Under these conditions the end-of-range regions are fully converted into highly porous silicon, which is more insulating and thus emits fewer secondary electrons, appearing darker than the surrounding lower porosity silicon for the 17 μm width irradiated area shown in Fig. 3b. After mild oxidation and immersion in dilute HF, all high-porosity silicon at the end-of-range regions was removed (Fig. 3c). This process created buried, hollow channels which can be cylindrical or rectangular in cross-section, depending on the irradiated surface width; the left-most channels with a line fluence of $\Psi_l = 3 \times 10^{10}$ cm^{-1} are perfectly cylindrical with ~1 μm diameter, whereas those formed by extended width irradiation have a uniform height which is determined by the depth extent (2 μm) of the high defect density peak at the end-of-range region (Fig. 1a).

Depending on the required channel dimensions, aspect ratio and depth below the surface, one may not want or need to form completely hollow channels. For example, in Fig. 3d, a higher fluence irradiation of 1×10^{15} ions cm^{-2} over a width of 1 μm was used to fabricate buried channels containing a large core which occupies most but not all of the available channel volume. A hollow channel is located above the solid core, with a height of only 100 nm and a width of about 1.2 μm. Nanoslit channels formed in this manner are significantly more asymmetric than those containing no solid core, such as those shown in Fig. 3c.

Fig. 3e shows how smooth-walled, vertical channels were produced using a high line fluence ($\Psi_l = 6 \times 10^{11}$ ions cm^{-1}) irradiation with 1 MeV protons, focused to a line width of 200 nm on the wafer surface. A high line fluence is needed so that the low defect density region extending from the surface to the end-of-range region is sufficiently damaged to form highly porous silicon upon anodization, which should be stopped before the formation of a large silicon core at the end-of-range depth shown in Fig. 3e. Fig. 3e also shows a higher magnification of these vertical channels extending from the surface to a depth of ~5 μm in which the ability to vary the channel width by altering the line fluence is seen (the right-most channel having a width of about 400 nm). The use of a higher proton energy of 2 MeV (range of 50 μm) enables fabrication of such vertical channels of widths about 1 μm and depths of 40 μm. Fig. 3f shows how channels may be fabricated at different depths using two proton energies: 500 keV (range of 7 μm), $\Psi_a = 1 \times 10^{14}$ cm^{-2}, and 400 keV (range of 5 μm), $\Psi_a = 4 \times 10^{13}$ cm^{-2}. The resolved highly porous regions at the two end-of-range depths are clearly seen and easily defined by the proton energy.

Regarding the uniformity of the porous silicon channel width and roughness along their lengths, we consider that this will be in the order of ±10 nm based on previous results of forming silicon wires with a higher line fluence,[55,59] but otherwise a similar fabrication process as described here.

Fig. 4a shows the same 10 μm wide hollow channels in porous silicon as in Fig. 3c. After oxidation to convert porous silicon into FOPS, the increased transparency and smooth, crack-free surface of the glass and the channels are clearly seen. Centimeter-long, smooth channels of micrometer dimensions were fabricated using the same process.

In Fig. 4b, c a lower proton beam energy of 100 keV (range of 850 nm in silicon) was used to fabricate nanochannels. Lower energy ions undergo less multiple scattering so the extent of high defect density peak at the end-of-range region is less (FWHM ~160 nm) than at higher ion energies, resulting in hollow channels of ~90 nm diameter, as pointed by an arrow in the central image, and rectangular channels with a height of ~100 nm, the left-most image. In the right-most of the three images, the three channels produced in porous silicon are ~400 nm wide and 150 nm high. The fluence of $\Psi_l = 2 \times 10^9$ cm^{-1} is ten times less than that of the channels fabricated with 1 MeV protons shown in Fig. 3c, also a consequence of reduced lateral scattering. The right-most image in Fig. 4b shows the same three channels in glass (within the dashed ellipses) after high temperature oxidation of the porous silicon. Although this image is a little blurred owing to charging problems, in this example clearly the channel dimensions are reduced after oxidation by approximately 100 nm. There are a variety of factors which can contribute to this, which are related to porosity, oxidation time, profile and temperature.[63] However, this same effect has the potential to shrink larger channel dimensions towards nanoscale dimensions. Fig. 4c shows an optical micrograph of the same array of nanochannels in glass.

Fig. 4d, e present examples of more complex channel geometries formed in glass using 1 MeV protons, showing a Y junction where two narrow channels (5 and 10 μm) join to form a wider channel, and wide channels tapering to micron diameter channels, with different taper profiles.

4. Integration of channels with large scale components

We explored several processes for integrating buried channels in porous silicon and glass with larger scale structures such as fluid reservoirs using existing methods of surface patterning of porous silicon. Here we present two examples and describe

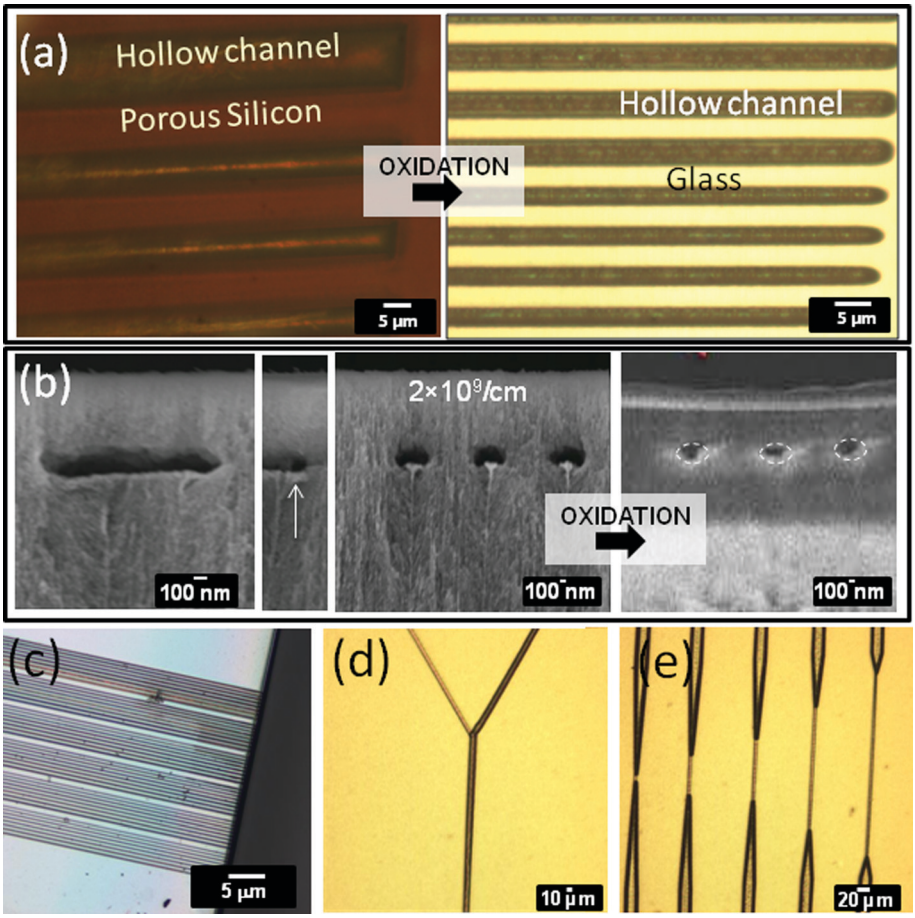

Fig. 4 (a). Plan-view optical micrograph of the same 10 μm wide hollow buried channels shown in Fig. 3c, before and after oxidation. (b) Similar process using 100 keV protons for [left] a 100 nm high rectangular channel in porous silicon, [center] 90 nm diameter channels (pointed by the arrow), [right] three channels at $\Psi_l = 2 \times 10^9$ cm^{-1}. The same three channels in glass after oxidation are shown in the right-most image, located by the three dashed ellipses. (c) Plan-view optical micrograph of the same glass channel array as in (b). Complex glass channel geometries shown in (d) a Y junction and (e) different profiles of tapered channels.

which is best suited to combine with channels in porous silicon and glass to produce a structure shown in Fig. 5a.

First, laser exposure[14] results in oxidation of the porous silicon in a manner similar to that described in section 2, allowing exposed areas to be selectively removed. An example of its use to produce a wide surface channel is shown in Fig. 5b, using a 532 nm laser to expose the surface of porous silicon with a spot size of 10 μm. Integration with sub-surface channels may be achieved by first using ion irradiation to pattern channels, followed by anodization to form porous silicon. After a suitable period of time to allow the highly porous silicon at the end-of-range regions to be oxidized, the surface is selectively exposed to the laser to define the reservoirs. Buried channels and reservoirs are finally formed in the same step of immersion in dilute HF (Fig. 5b). The location of connecting micrometer-diameter buried channels is indicated, though it is difficult to see beneath the opaque porous silicon surface. One drawback of this process is that the laser exposure time required to make large reservoirs is hours long, and since the exposed depth is limited to about 10 μm (Fig. 5b), then one may need to etch and re-expose the reservoirs in order to make them deeper. Furthermore, the process is sequential so it is not feasible for wafer-scale fabrication, and alignment is not easy because one cannot easily see the locations of the buried channels.

Fig. 5c shows reservoirs made by etching a masked silicon surface in KOH. A patternable polymer, Protek, was used to mask those areas of the surface where no etching was required. One obvious feature of this process is that the reservoirs have sloping sidewalls owing to the characteristic feature of KOH etching of silicon where atoms on {111} planes which are aligned at 55° to the [001] surface etch slowly. This makes subsequent formation with buried channels difficult as the sloping sidewalls result in the end-of-range region changing in height across the angled sidewall.

Fig. 5d shows a similar structure made using a different process. Here the silicon wafer was first patterned with reservoirs using reactive ion etching (RIE) to a depth of 20 μm. This process has the advantage of wafer-scale fabrication using standard equipment, allowing many samples to be produced simultaneously. Buried channels are then fabricated between two reservoirs by irradiation, anodization and oxidation. Since the

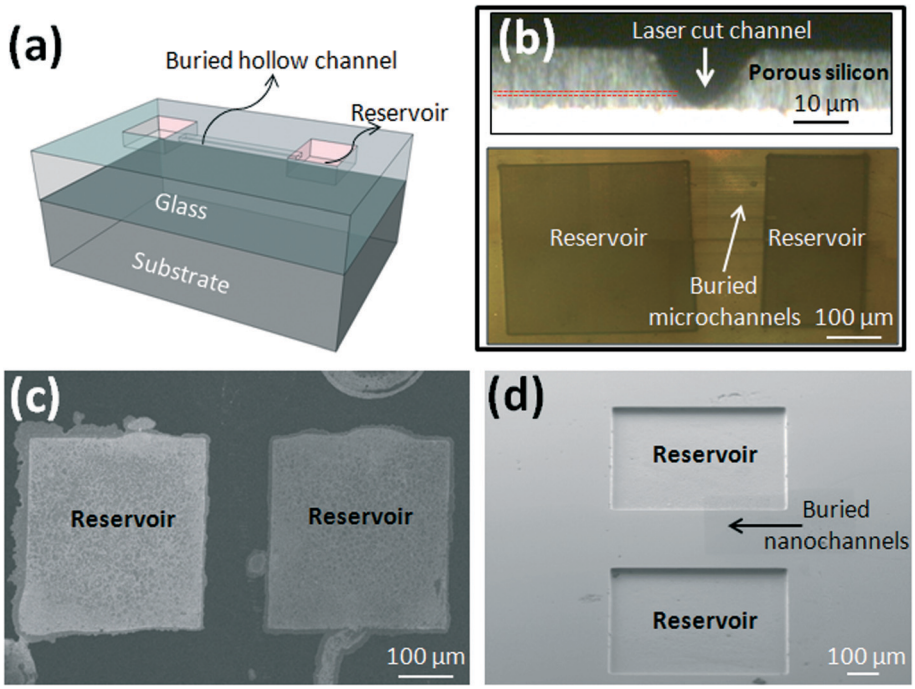

Fig. 5 (a) Schematic of buried hollow channels connected to large reservoirs. (b) [Upper] Cross-section of channels in porous silicon formed by laser-induced oxidation. [Lower] Device where hollow microchannels in porous silicon are connected to reservoirs formed by laser oxidation. (c) Reservoirs in silicon formed by KOH etching. (d) Device where nanochannels in glass are connected to reservoirs formed by RIE and FIB.

reservoirs are easy to see, accurate location of the channels is easily achieved. However, there is one remaining problem with this process: the zone where the buried channel meets the reservoir is not well-formed owing to the thin damaged layer produced by RIE. Since the whole purpose of ion irradiation is to produce a well-defined volume of damage at the end-of-range region, any other damage to the silicon lattice will alter the manner in which anodization current flows around this zone, resulting in the channel not properly opened. This can be solved by using a gallium focused ion beam (FIB) to mill away the improperly formed zone, exposing hollow channels to the reservoir; those shown in Fig. 3d were exposed in this manner, requiring a milling time of ~15 minutes.

5. Studies of DNA extension in buried glass channels

PDMS is the most popular fabrication method for such nanochannel studies of DNA flow. In comparison, our process offers the ability to fabricate high aspect ratio nanostructures, as well as regular-shaped ones such as circular channels (Fig. 3). Furthermore, since the material is either porous silicon or glass, the chip is bio-friendly, allowing biomedical and biological studies. For the same reason, the chip is reusable, thus eliminating the effect caused by different configurations.

Bacteriophage T4-DNA (166 kbp) was purchased from Nippon Gene, Tokyo and used without further purification. Fluorescence dye YOYO-1 was purchased from Invitrogen, Carlsbad, CA. T4-DNA was stained with YOYO-1 with a maximal intercalation ratio of 4 base-pairs per dye molecule. The dye-corrected contour length of the stained DNA molecules amounted to 73 μm. Samples were prepared by dialyzing solutions of DNA against 10 mM Tris–HCl in microdialyzers. The Tris–HCl concentration is 10 mM (Tris adjusted with HCl to a pH of 8.0), *i.e.*, 2.9 mM TrisCl and 7.1 mM Tris. The DNA concentration is 0.003 g L^{-1}. No anti-photobleaching agent was used.

The solution of the stained DNA molecules was loaded into the two reservoirs connected by the buried channels (Fig. 5d). The glass channels are nanoslits with a rectangular cross-section of 100 by 1200 nm. DNA molecules were subsequently driven into these nanoslits by electrophoresis. This was achieved using two platinum electrodes immersed in the reservoirs and connected to an electrophoresis power supply with a voltage of 1 V (Keithley, Cleveland, Ohio). DNA molecules localized inside the channels were visualized using a Nikon Eclipse Ti inverted fluorescence microscope equipped with a 200 Watt metal halide lamp, a filter set, and a ×100 oil immersion objective. The exposure time was controlled by a UV light shutter. After switching off the electric field, the molecules were allowed to equilibrate for at least 60 seconds. Images were collected using an electron multiplying charge coupled device (EMCCD) camera (Andor iXon X3), and the extension of the DNA molecules along the direction of the nanoslits was measured using the ImageJ software (http://rsb.info.nih.gov/ij/). During the visualization process there is no obvious photocleavage or change in extension.

A fluorescence image as well as an intensity profile of T4-DNA molecules confined in the array of nanoslits in glass is shown in Fig. 6. The average extension is 17 ± 2 μm, which is about 25% of the contour length. A similar extension has

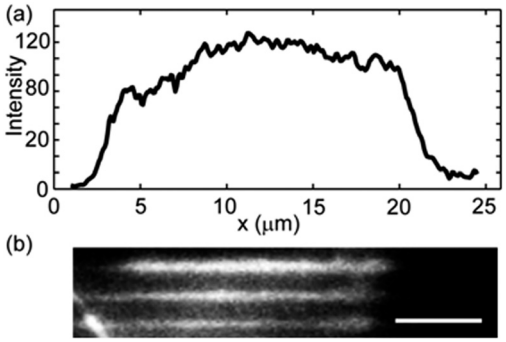

Fig. 6 (a) Fluorescence intensity profile along the channel of the top molecule in panel b; (b) fluorescence image of T4-DNAs confined in an array of 100 by 1200 nm nanoslits. The scale bar denotes 5 μm. The average DNA extension is 17 ± 2 μm.

been reported previously for DNA at similar ionic strength and confined in 100 by 1000 nm nanoslits fabricated in PDMS resin.[59] We note that several DNA molecules are simultaneously accommodated in the array of channels and all are linearized to approximately the same extension.

6. Conclusions

In conclusion, we have developed a technique for fabricating multilevel, micro- and nanoscale buried channels in porous silicon and glass and demonstrated how they can be integrated with larger scale features to provide structuring of these materials over length scales of millimeters to ~100 nm. We consider that a value of about 100 nm represents the present level of certainty and control of the channel dimensions, largely governed by the oxidation step. A porous silicon grain size of about 30 nm (Fig. 3a) imposes further limitation, which one may be able to overcome by choosing more optimized anodization conditions.

Further work is being conducted to demonstrate the ability to fabricate vertical channels which connect horizontal channels at one or more depths, at which point this process may offer a route to develop densely-packed 3D channel architectures. We believe this capability will provide the means to significant developments in fields such as nanofluidics, lab/systems-on-a-chip technologies and sensing.

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